Remarks

As best as Applicant can understand the generalized explanations in the Final Office Action, Applicant submits that the record shows plain and clear error in interpreting the claims and the asserted references and in unsuccessfully attempting hindsight reconstruction from complex portions of circuits in three different references. The impropriety of the § 103(a) rejection (Schmoock '994 in view of Valley '779 and AAPA) is so clear that no attempt has been made to explain how the circuits in three references could possibly be combined to reconstruct a corresponding embodiment.

To highlight some of the misunderstandings, Applicant had asked the Examiner to explain this strange combination of teachings in light of the Examiner's previous acknowledgement that the Valley '779 reference does not monitor over-current protection scheme. In the instant Office Action's Response to Arguments, after mischaracterizing Applicant's written arguments, the Examiner now erroneously argues (without any support or cites) the rejection "since Valley ['779] also monitors over-current protection scheme." Not only does the Valley '779 reference fail even to mention any kind of over-current protection, the Valley '779 reference clearly teaches that it is directed to over-voltage protection using a current supply that is fixed (*e.g.*, Col.3:21-43). Moreover, the pending rejection indicates that the asserted combination of teachings is basically an insertion of the entire over-voltage protection circuit of Fig. 1 of the Valley '779 reference somehow into the over-voltage protection circuit of Fig. 2 of the Valley '779 reference (and fitting in somewhere the comparator shown in AAPA) for the purpose of implementing a (yet to be identified) form of over-current protection "in order to defect a fault" (p.6 of Final Office Action). This combination of teachings is so illogical that a skilled artisan would not be motivated to modify the Schmoock '994 reference as the Examiner proposes; under the law, inoperability is strong evidence that the cited references teach away from the modification. See M.P.E.P. § 2143.01(V). Consistent therewith, the Supreme Court in *KSR* explained that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007).

Applicant believes that the Section 103 rejections are improper for reasons stated in Applicant's responses of record, which are fully incorporated herein by reference. Generally, Applicant believes that the Examiner has misread claim 1 and improperly ignored the claim limitation, which is present in the claim terms recited in claim 6. The Office Actions of record have therefore improperly asserted that the features upon which applicant relies are not present in the rejected claims. Furthermore, in addition to attempting to ignore claim limitations with "intended-use" assertions, the asserted combination fails to present correspondence in connection with both a comparator and a feedback/measurement circuit as set forth in claims 1 and 6.

These and other problems with the rejection have been previously explained (herein incorporated by reference) and are supplemented in the discussion below (in which Applicant does not acquiesce to averment unless expressly indicated).

The Final Office Action fails to explain how the § 103(a) rejection is being asserted in a manner that would not undermine the purpose of the '994 reference. *See* M.P.E.P. § 2143.01. Without any discernible explanation that explains how these circuits are being combined and from which references the missing claimed elements are being extracted, the Examiner alleges an argument that is conditional. In the Final Office Action at p.3, the Response to Arguments explains that the purpose of the Schmoock '994 reference would not be undermined because "it would be possible to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value without rendering Schmoock unsatisfactory for its stated purpose." There is no explanation for why or how this problematic condition would arise and/or in what proposed circuit such a condition would arise. Should this rejection be maintained, Applicant again requests clarification and compliance with M.P.E.P. § 7070(f).

Applicant maintains its position previously presented. According to the rejection, the '994 reference discloses a comparator (*i.e.,* element 40 of Figure 2) that compares the voltage of the source of transistor 32 to the voltage of the source of transistor 52; however, the Examiner acknowledges that the '994 reference does not teach that this "comparator" outputs a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs as in the claimed

invention. The Examiner then proposes modifying the '994 reference's operational amplifier 40 such that it outputs a low-current signal. Applicant submits that such a modification would render the '994 reference unsatisfactory for its stated purpose of providing an over-current protection scheme that protects switch transistor 32. *See, e.g.,* Figure 2 and Col. 5:8-11. Specifically, the '994 reference's operational amplifier 40 adjusts its output signal in relation to the differential signal at its inputs in order to cause the source voltages of transistors 32 and 52 to be relatively equal, thereby providing over-current protection. *See, e.g.,* Figure 2 and Col. 6:35-50. The Examiner's proposed modification would alter the '994 reference's operational amplifier 40 such that it would output a low-current signal (responsive to the voltages on the outputs of the transistors 32 and 52), instead of adjusting its output signal to control the source voltages of the transistors 32 and 52 as required by the '994 reference to provide over-current protection. Applicant submits that the '994 reference's operational amplifier 40 would no longer provide over-current protection, thus rendering the '994 reference unsatisfactory for its stated purpose. As such, there is no motivation for the skilled artisan to modify the '994 reference in the manner proposed by the Examiner.

Applicant also fails to appreciate the Examiner's position with respect to page 3:5-13 of the instant Office Action where the Examiner confuses the level of the signal output by operational amplifier 40 (*e.g.,* a low output) with what kind of output signal is being produced by the operational amplifier 40 (*i.e.,* an output signal that controls the source voltages of the transistors 32 and 52). Applicant submits that a low (level) output signal is not equivalent to a low-current signal (which could be a low level or a high level signal) that is produced responsive to comparing the voltages across main cell and sense cell outputs. Irrespective of the level of the output signal generated by operational amplifier 40, the Examiner's proposed modification would result in operational amplifier 40 generating a low-current signal responsive to comparing the voltages on the outputs of the transistors 32 and 52, instead of adjusting its output signal in relation to the differential signal at its inputs in order to cause the source voltages of transistors 32 and 52 to be relatively equal. As such, the Examiner's proposed modification would render the '994 reference unsatisfactory for its intended purpose of providing over-current protection using operational amplifier 40.

Accordingly, the § 103(a) rejection of claims 1-7 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-7 because the cited combination does not correspond to the claimed invention which includes, for example, aspects directed to comparing the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs. The Examiner acknowledges that the '994 and '779 references fail to disclose a comparator that outputs a low-current signal as in the claimed invention. The Examiner then cites to the comparator 18 of Applicant's Figure 1 (admitted prior art) and fails to explain where or how the citation to the AAPA's comparator would be implemented in the asserted hypothetical embodiment.

Applicant previously requested that the Examiner provide clarification regarding how the cited references are being combined, and while Applicant appreciates the Examiner's clarification that the '994 reference's feedback circuit (*i.e.*, elements V_{ref}, 44 and 48 of Figure 2) is being modified to provide both over-current protection and under-voltage protection, the Examiner still has not provided any detail regarding how the '994 reference's feedback circuit is to be modified or how the Examiner is modifying the feedback circuit of the '994 reference to provide two different protection schemes that are not taught as being provided together by the feedback circuits of either reference.

Applicant further submits that new claims 8-14 are allowable over the cited references for reasons including those stated above. Also note that new claim 8 largely tracks with method claim 6, and claim 1, and is distinguishable for the same reasons as discussed above.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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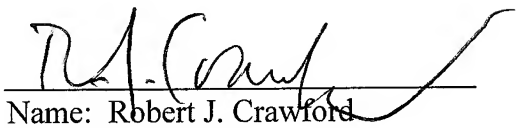
By: 

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